

# Topstar Digital technologies Co.,LTD

Board name: Mother Board Schematic

Project name: P51

Version: Ver B

Initial Date:

New update:

1. System Block Diagram & Schematic page description;

2. Power Block Diagram & Discription;

3. Annotations & information;

4. Schematic modify Item and history;

5. Power on & off Sequence;

6. ACPI Mode Switch Timings;

7. Power On Sequence Map;

8. CLOCK Distribution;

9. Power Distribution;

Topstar Confidential

Hardware drawing by:

Hardware check by:

EMI Check by:

Power drawing by:

Power check by:

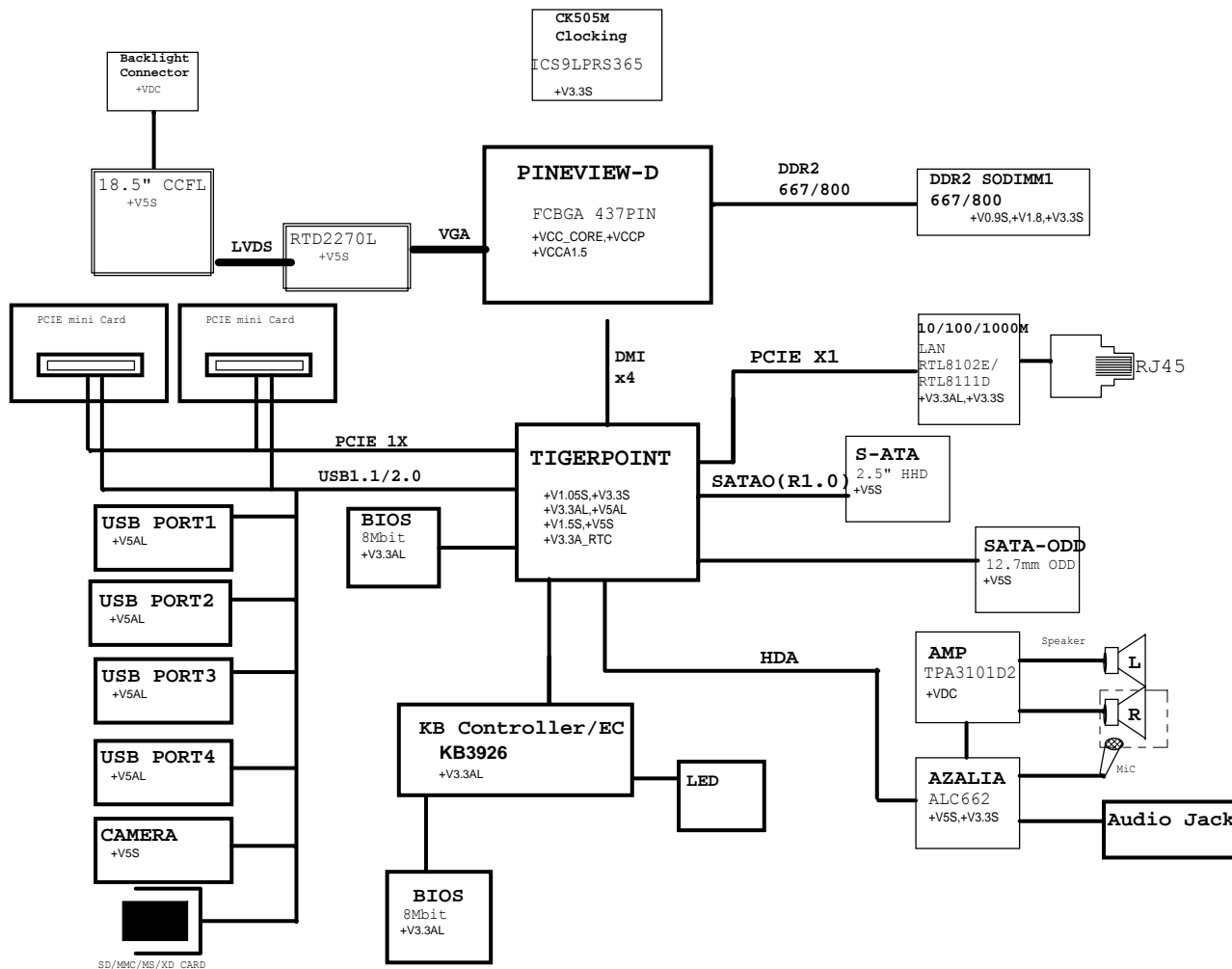
Manager Sign by:

<b>Topstar®</b>		TOPSTAR TECHNOLOGY	
Page Name		Title	
Size A3	Project Name PINETRAIL-D	Rev A	
Date: Thursday, April 01, 2010	Sheet 1 of 31		
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR.			

# Topstar Confidential

ShenZhen Topstar Industry Co.,LTD

N81 SYSTEM BLOCK Ver:A



Topstar®		TOPSTAR TECHNOLOGY	
Page Name		System Block & Index	
Size A3	Project Name	PINETRAIL-D	Rev A
Date:	Thursday, April 01, 2010	Sheet 2	of 31
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR			

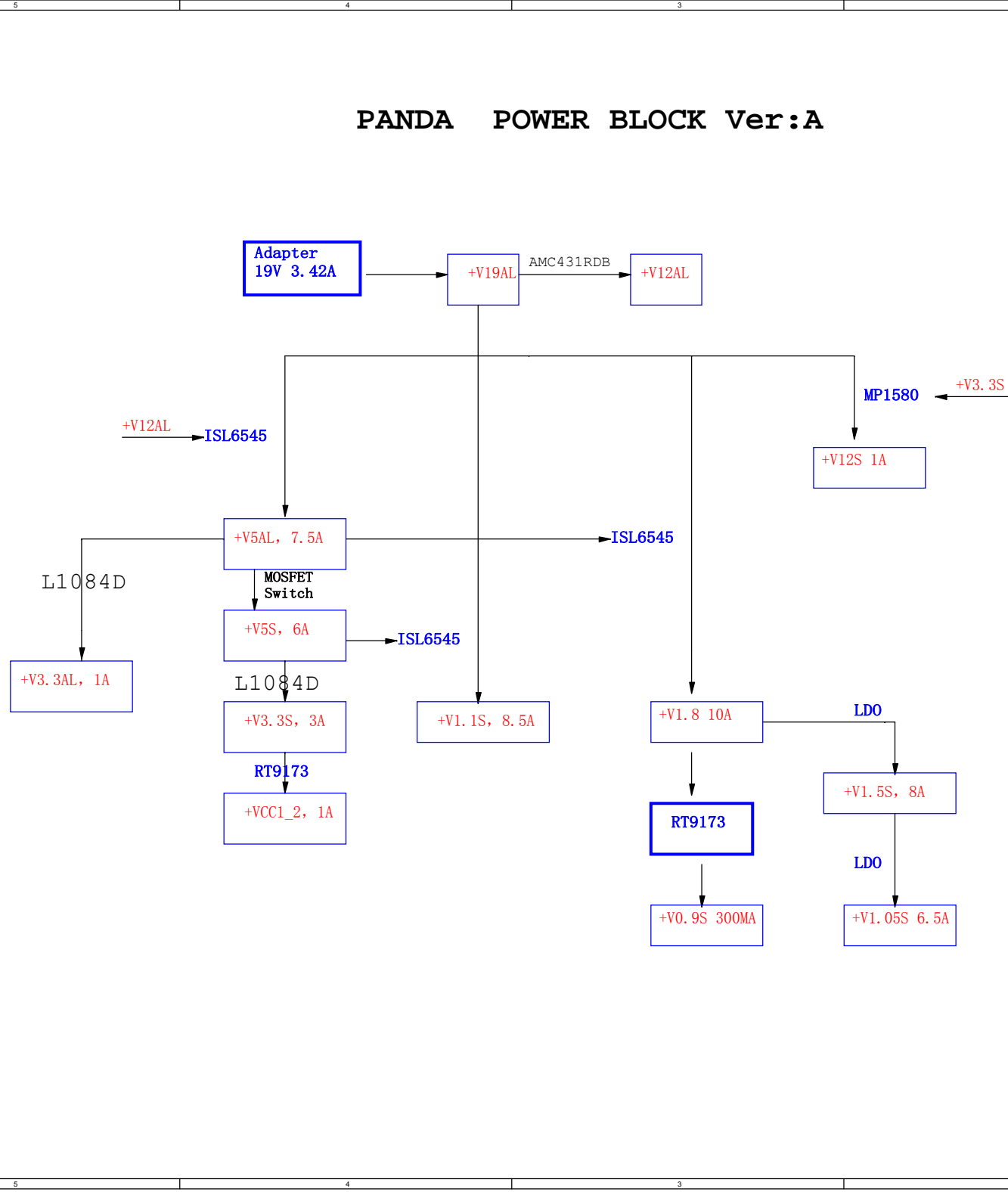
**PANDA POWER BLOCK Ver:A**

```
graph TD
    Adapter[Adapter 19V 3.42A] --> V19AL[+V19AL]
    V19AL -- AMC431RDB --> V12AL[+V12AL]
    V19AL --> V5AL[+V5AL, 7.5A]
    V19AL --> V11S[+V1.1S, 8.5A]
    V19AL --> V18[+V1.8 10A]
    V19AL --> V15S[+V1.5S, 8A]
    V19AL --> V12S[+V12S 1A]
    V12AL --> V12S
    V12AL -- MP1580 --> V12S
    V12AL --> V33S[+V3.3S, 3A]
    V12AL --> V33S1A[+V3.3AL, 1A]
    V12AL --> V33S1A
    V5AL -- MOSFET Switch --> V5S[+V5S, 6A]
    V5S -- L1084D --> V33S
    V5S --> V33S1A
    V33S -- RT9173 --> VCC1_2[+VCC1_2, 1A]
    V18 --> V09S[+V0.9S 300MA]
    V18 --> V105S[+V1.05S 6.5A]
    V15S -- LDO --> V105S
```

**Topstar®** TOPSTAR TECHNOLOGY

Page Name		PWR Block & description	
Size A3	Project Name	PINETRAIL-D	Rev A
Date: Thursday, April 01, 2010	Sheet	3	of 31

PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR.



Voltage Rails

+VDC	Primary DC system power supply (6V-9.5V)
+VBATTERY	Battery Power supply (6-8.4V)
VCCP	Core Voltage for CPU
+V1.05S	1.05V for Calistoga & ICH7M core / FSB VTT
+V1.8	1.8V power rail for DDR2
+V0.9S	0.9V DDR2 Termination voltage
+V3.3AL	3.3V always on power rail
+V5AL	5V for ICH7-M's VCC5 Refsus
+V3.3S	3.3V main power rail
+V5S	5V main power rail

Board stack up description

PCB Layers	Trace Impedence:55ohm +/-15%
Top(Signal1)	
VCC 2	
Signal 3	
Signal4	
Ground 5	
Bottom(Signal6)	

USB Table

USB Port#	Function Description
0	Standard USB2.0 Port
1	Standard USB2.0 Port
2	Standard USB2.0 Port
3	MINICARD USB
4	CAM USB
5	MINICARD USB
6	CR USB
7	NC

I2C SMB Address

Device	Address	Hex	Master
Clock Generator	1101 001x	D2	ICH7-M
SO-DIMMO	1010 000x	A0	ICH7-M
CPU Thermal Sensor	1001 100x	98	KBC
Smart Battery	0001 011x	16	KBC
PCIE Slot	TBD	TBD	ICH7-M

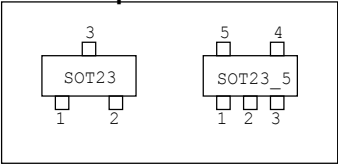
Power States

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*	+V*S	Clock
S0 (Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (STM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (STD)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SoftOff)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Wake up Events


LID switch from EC
Power switch from EC

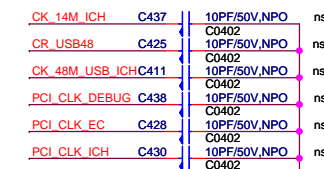
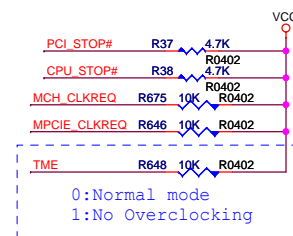
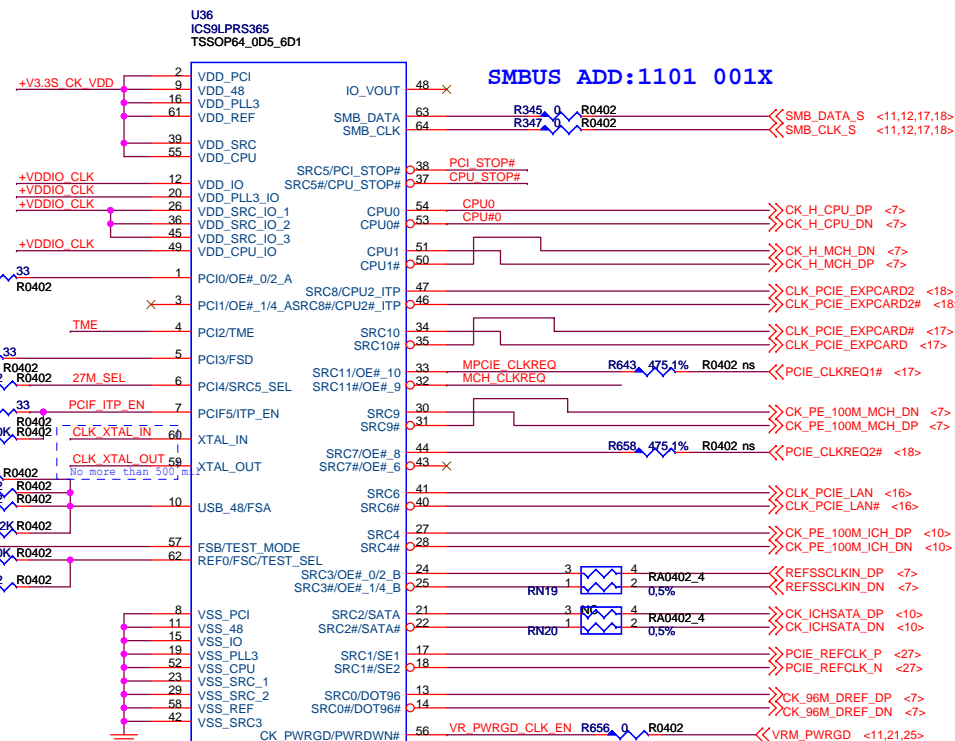
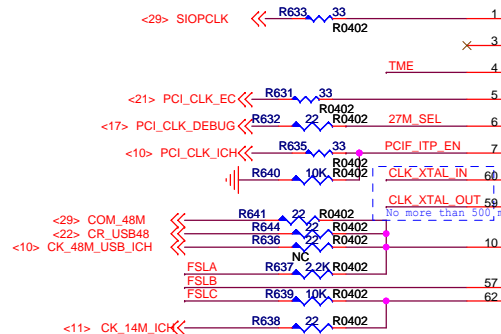
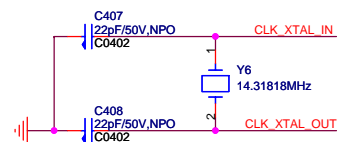
PCB Footprints

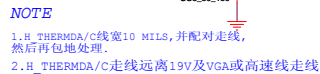
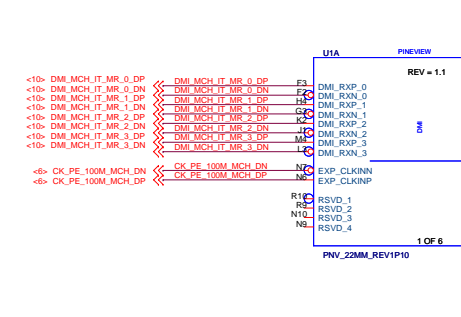
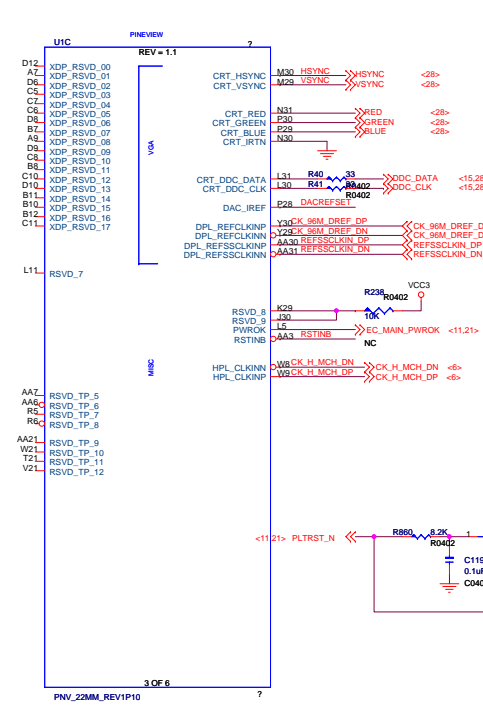


ns: Component marked "ns" is not stuff

Schematic modify Item and history:

		TOPSTAR TECHNOLOGY	
Page Name		Sch Modify and history	
Size A3	Project Name	PINETRAIL-D	Rev A
Date:	Thursday, April 01, 2010	Sheet	5 of 31
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR.			

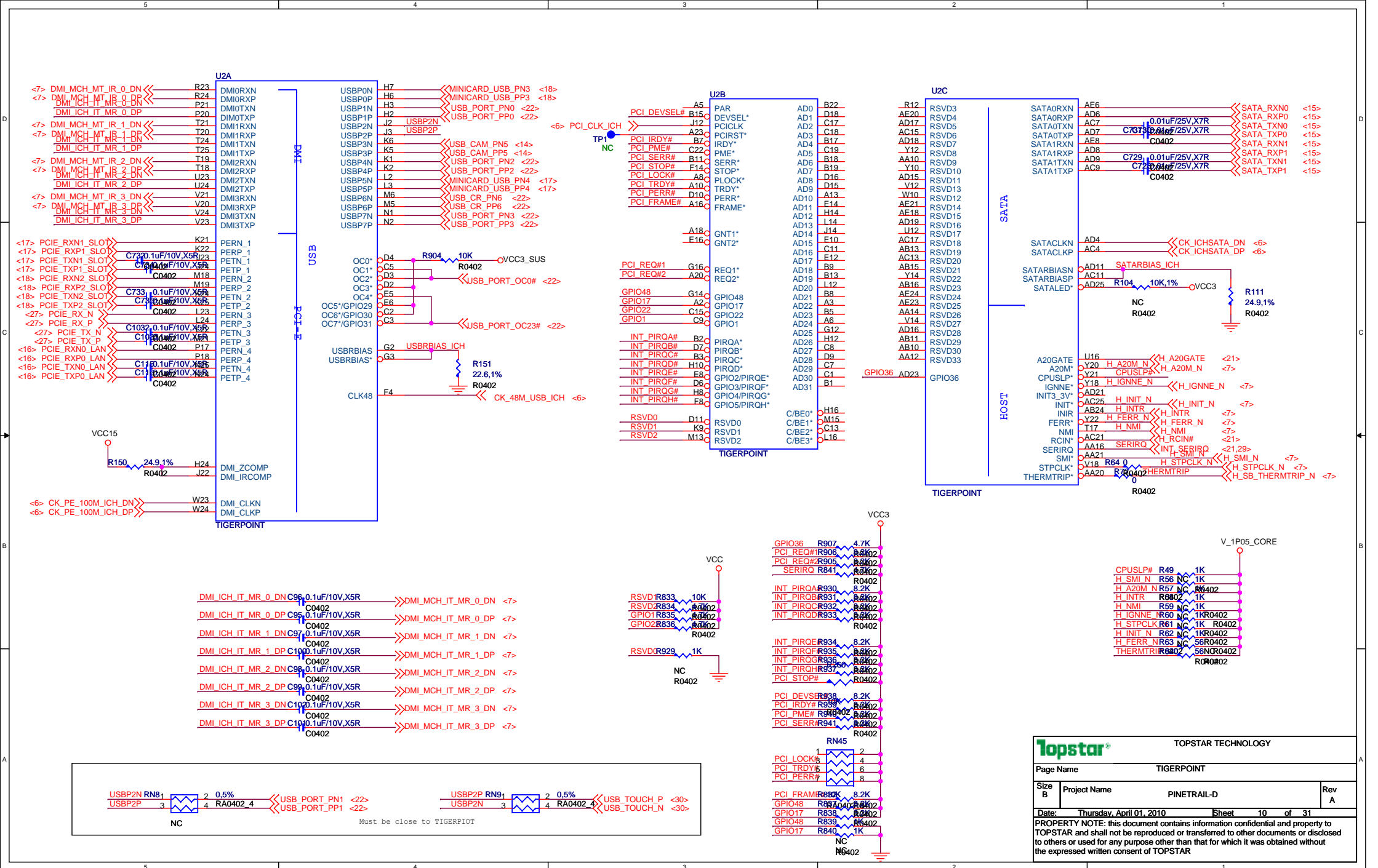




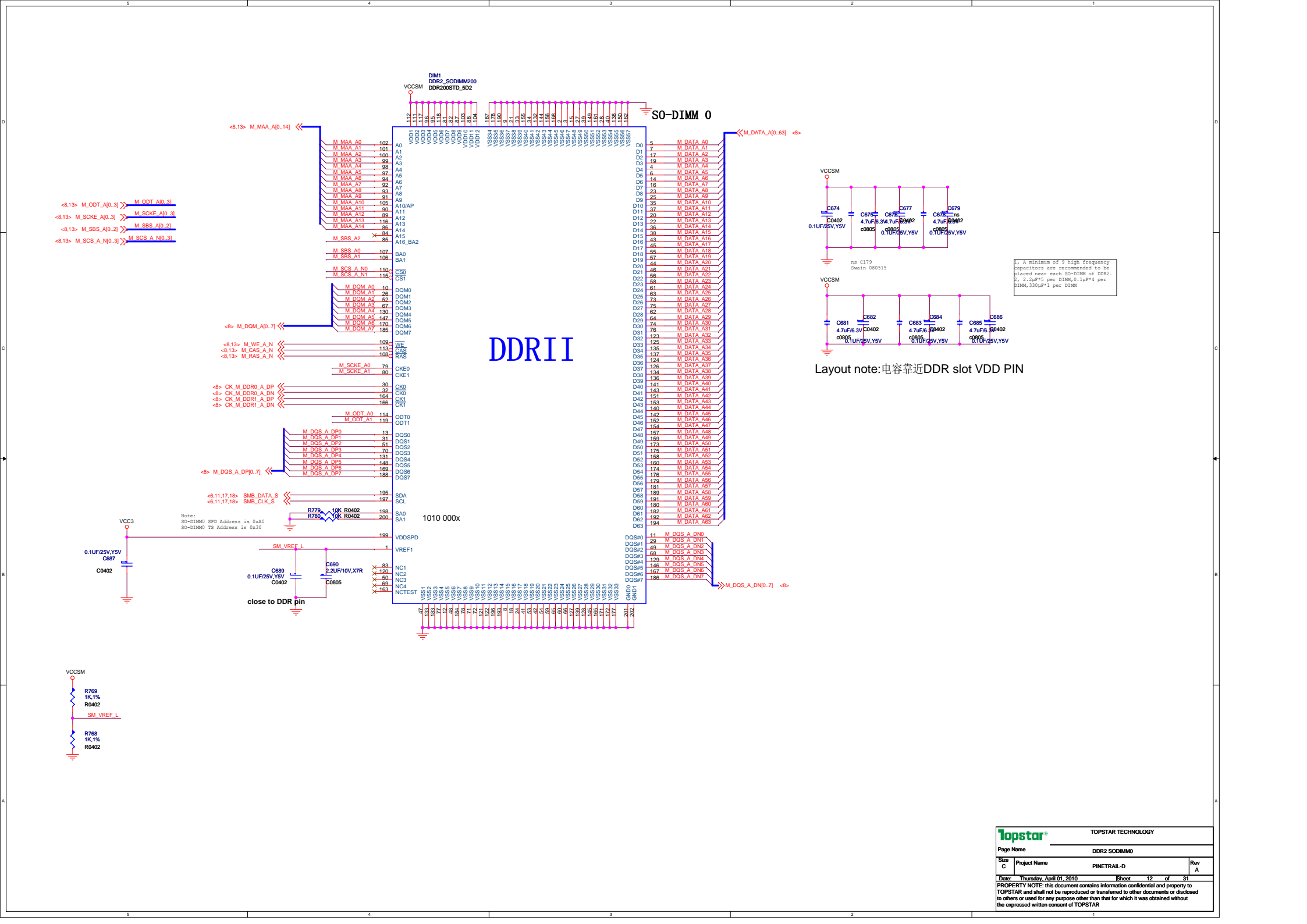




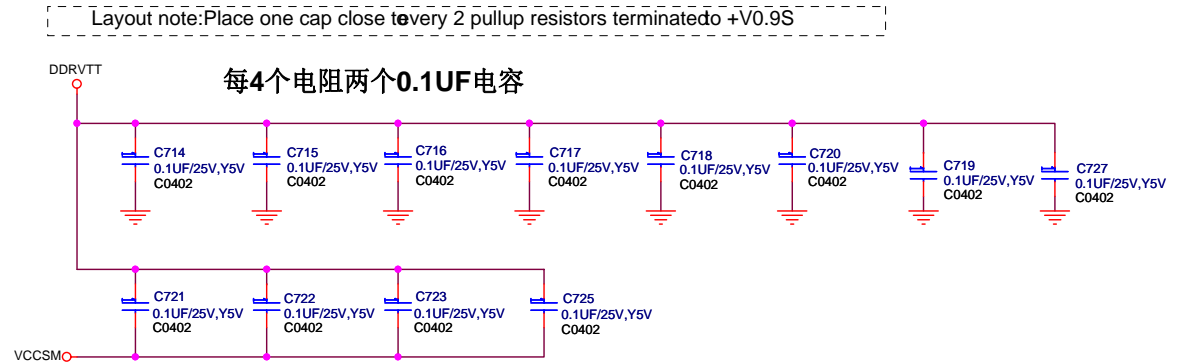
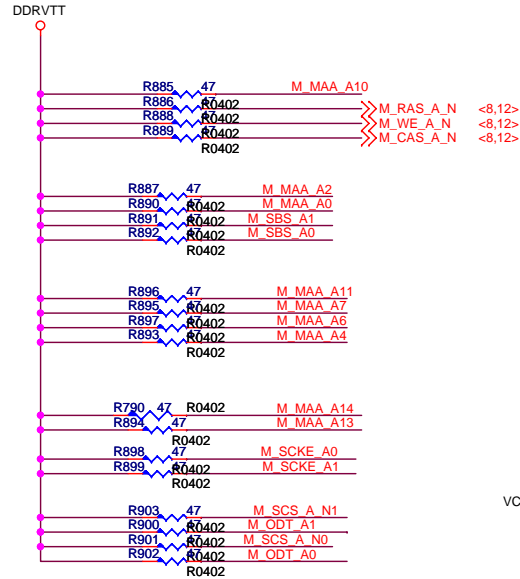
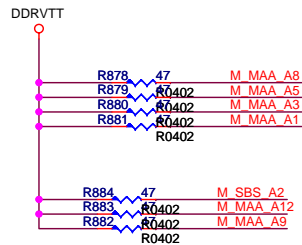




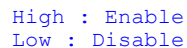




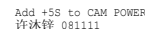
<8,12> M\_MAA\_A[0..14] << M\_MAA\_A[0..14]  
<8,12> M\_ODT\_A[0..3] <> M\_ODT\_A[0..3]  
<8,12> M\_SCS\_A\_N[0..3] <> M\_SCS\_A\_N[0..3]  
<8,12> M\_SBS\_A[0..2] <> M\_SBS\_A[0..2]  
<8,12> M\_SCKE\_A[0..3] <> M\_SCKE\_A[0..3]



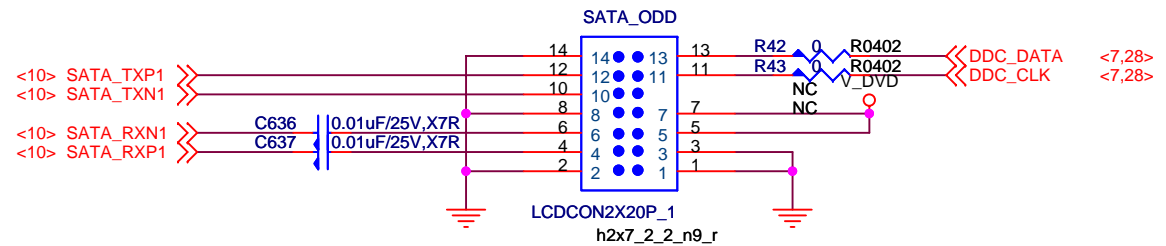
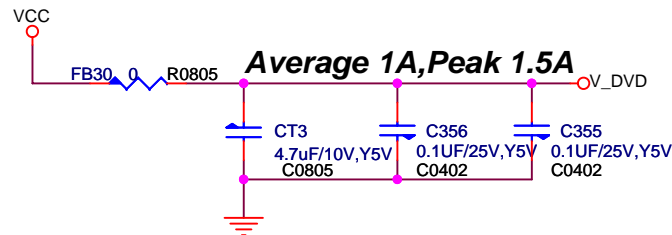
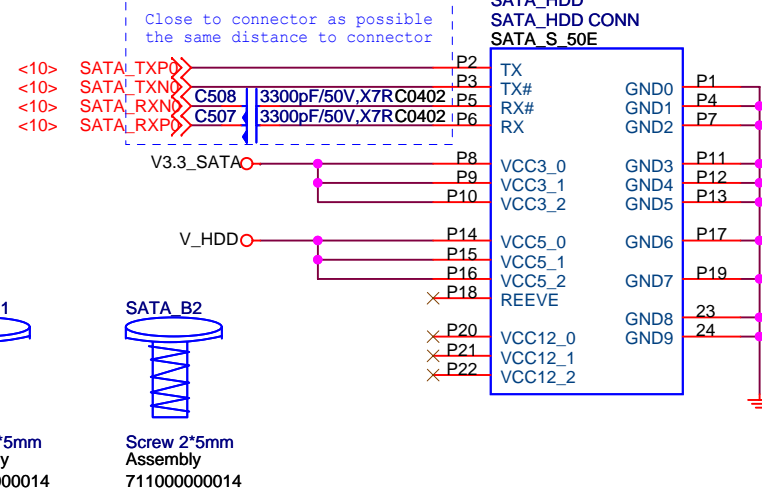
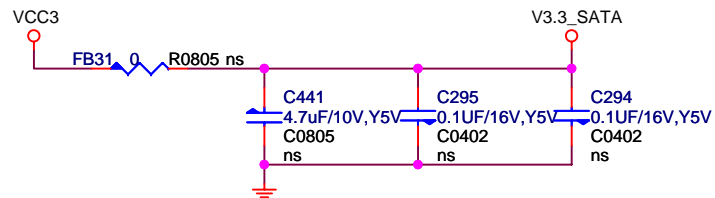
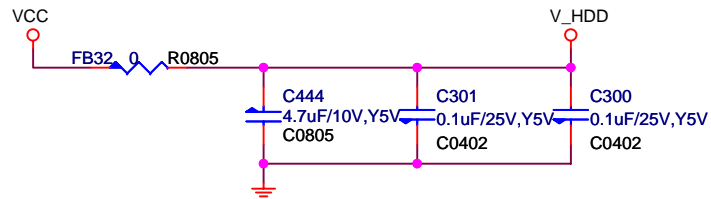
<b>Topstar</b> <sup>®</sup>		TOPSTAR TECHNOLOGY	
Page Name		DDR2 TERM and Decoupling	
Size B	Project Name	PINETRAIL-D	Rev A
Date: Thursday, April 01, 2010		Sheet 13 of 31	
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR			



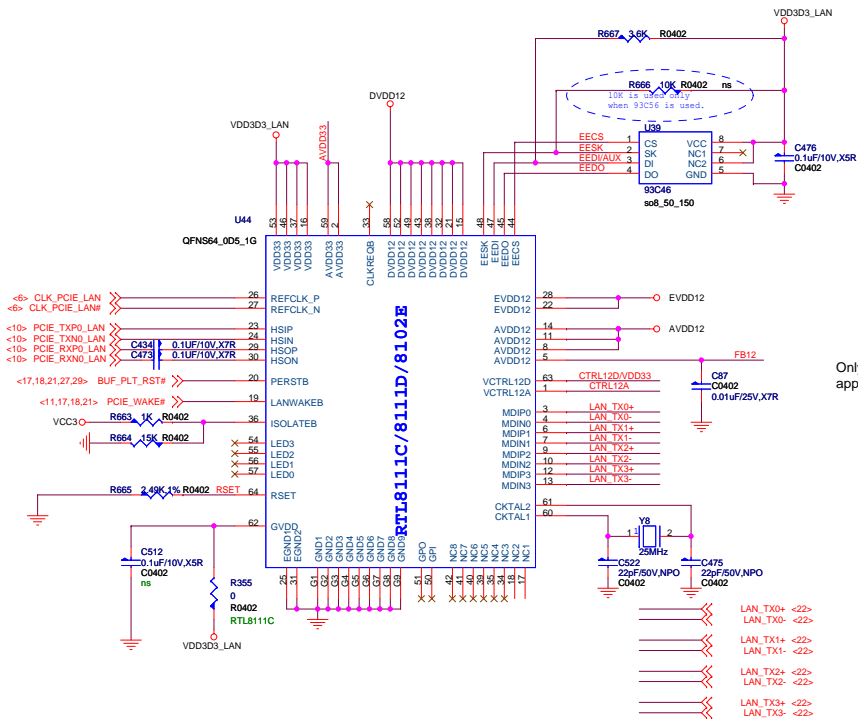
```
update LVDS_VDDEN to LOW active
090511
```



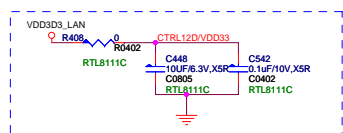
## SATA HDD





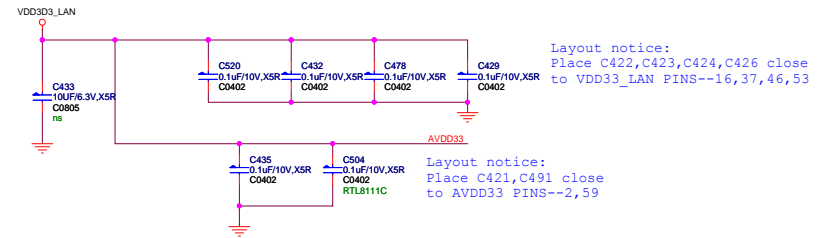
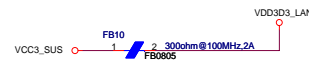
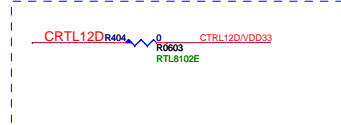


For RTL8111C(P), use this block.



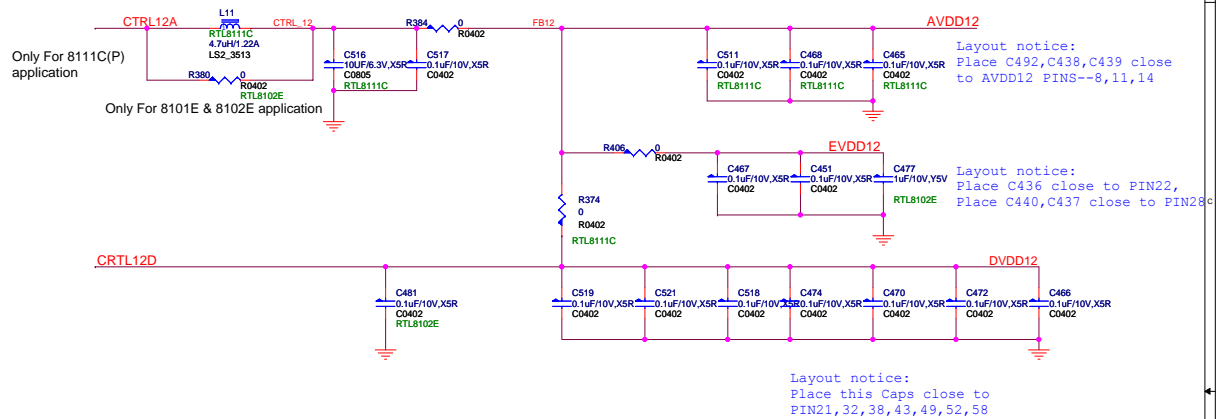
Layout notice:  
CTRL12/VDD33 should be wider than 40mil  
C447,C541 should be placed within 200mil of pin 63

For RTL8102E, use this block.



Layout notice:  
Place C422,C423,C424,C426 close  
to VDD33\_LAN PINS--16,37,46,53

Layout notice:  
Place C421,C491 close  
to AVDD33 PINS--2,59



Layout notice:  
Place C492,C438,C439 close  
to AVDD12 PINS--8,11,14

Layout notice:  
Place C436 close to PIN22,  
Place C440,C437 close to PIN28

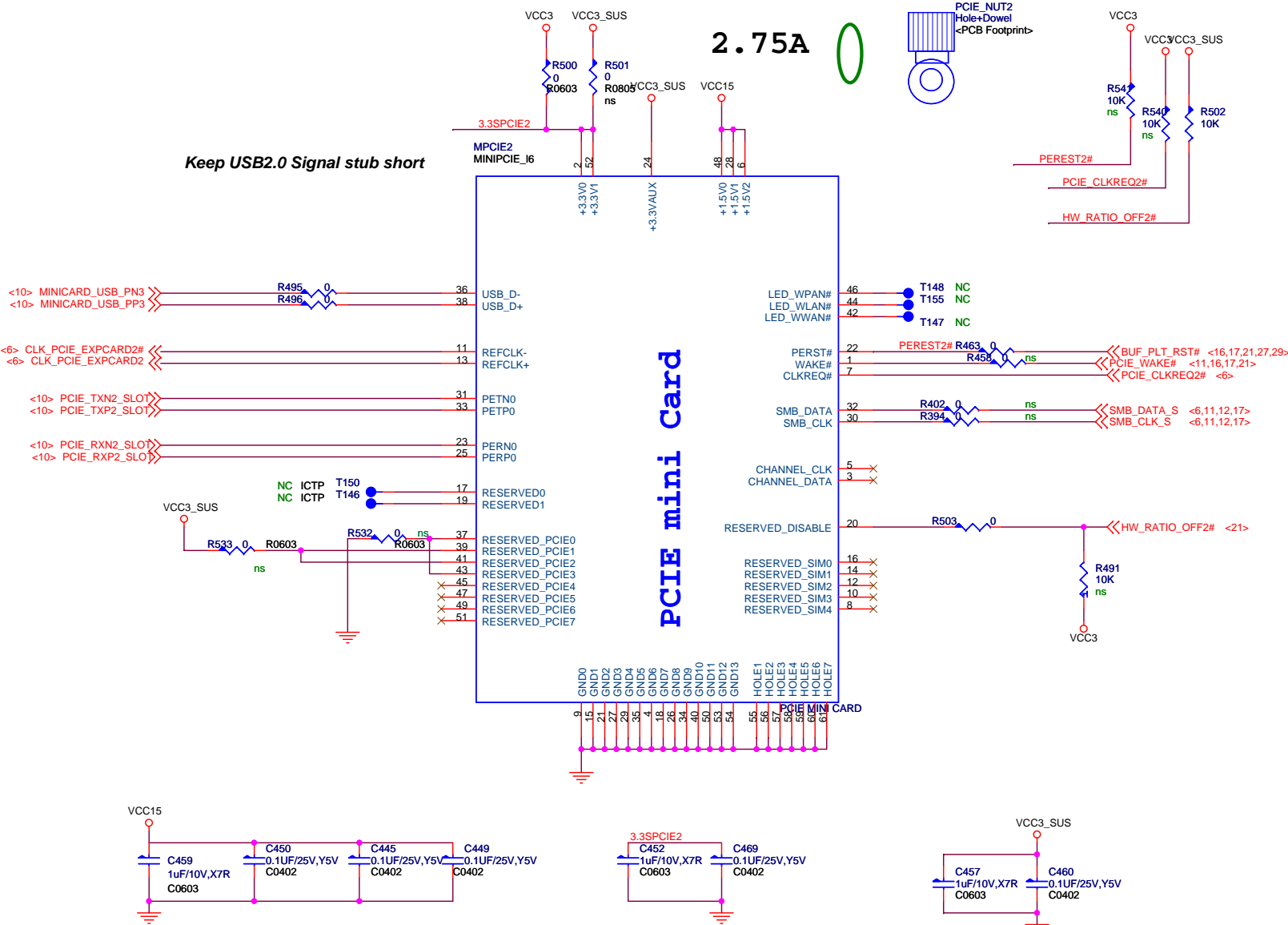
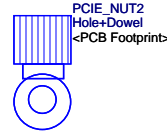
Layout notice:  
Place this Caps close to  
PIN21, 32, 38, 43, 49, 52, 58



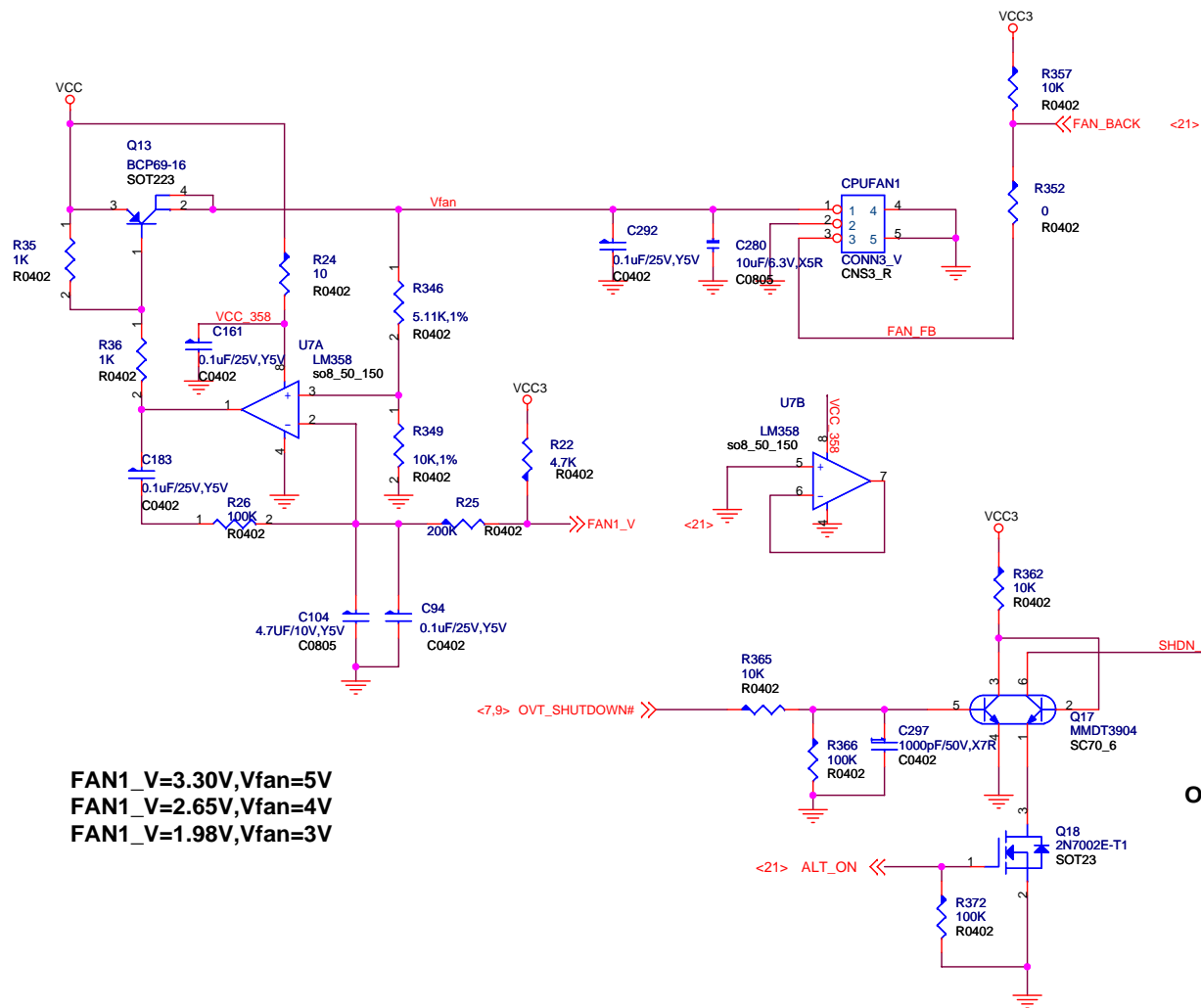


Keep USB2.0 Signal stub short

2.75A

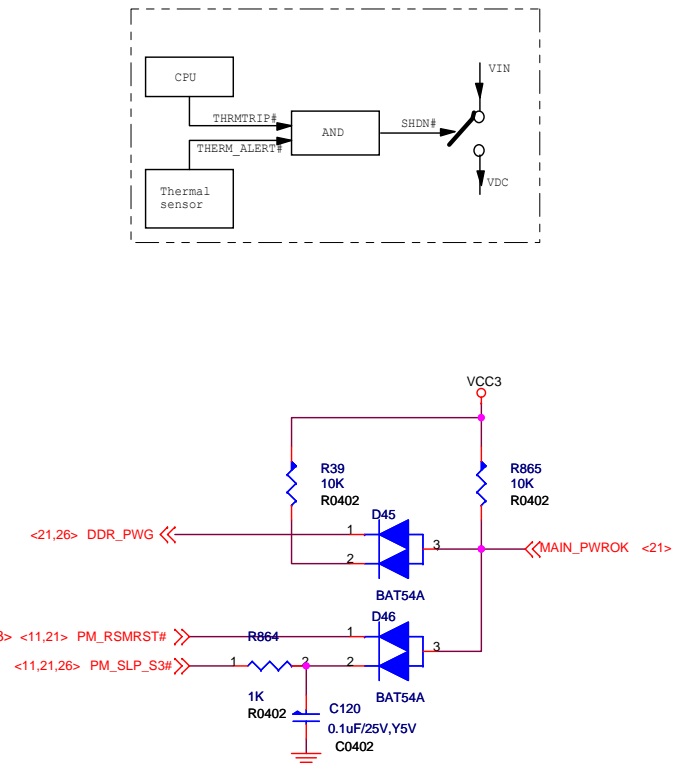



TOPSTAR TECHNOLOGY	
Page Name	
PCIE SLOT	
Size	Project Name
B	PINETRAIL-D
Rev	A
Date:	Thursday, April 01, 2010
Sheet	18 of 31
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR	



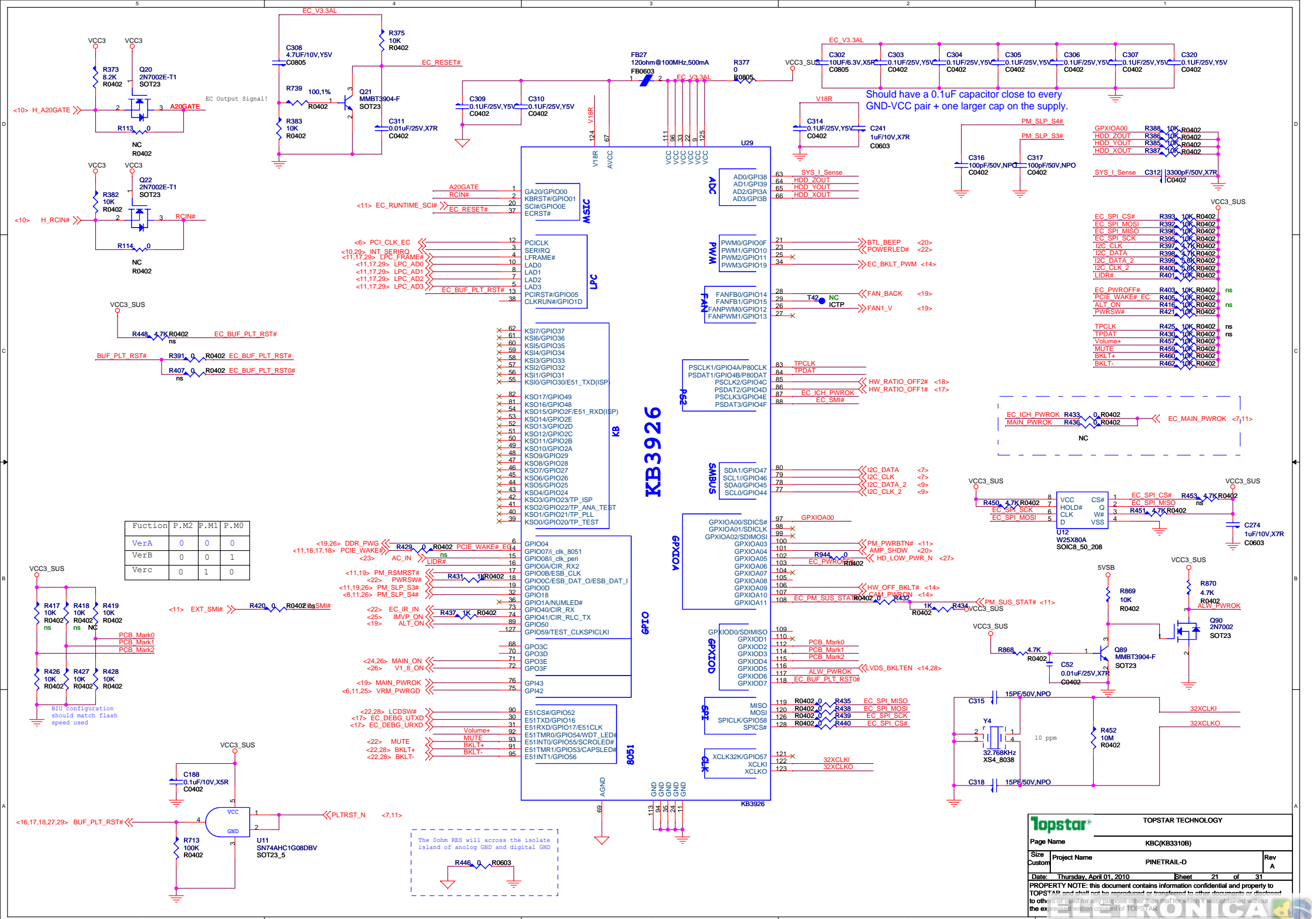
FAN1\_V=3.30V,Vfan=5V  
FAN1\_V=2.65V,Vfan=4V  
FAN1\_V=1.98V,Vfan=3V

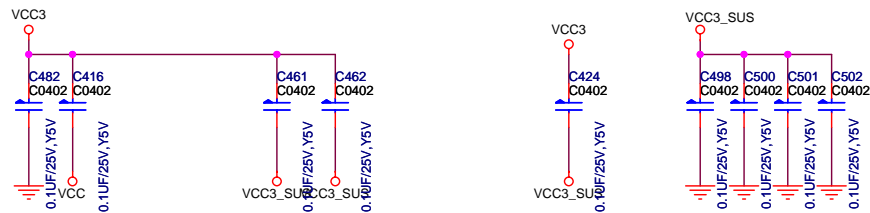
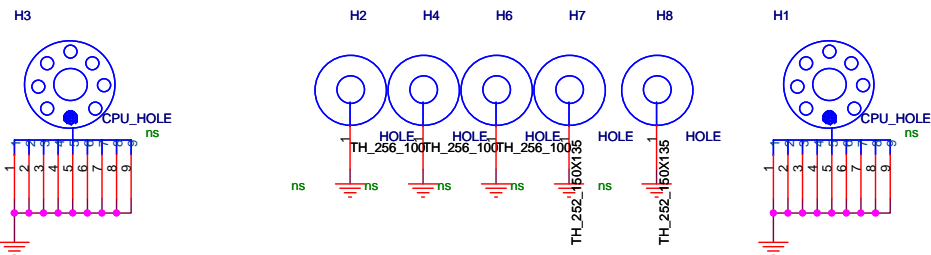
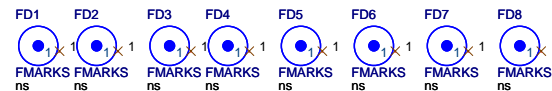
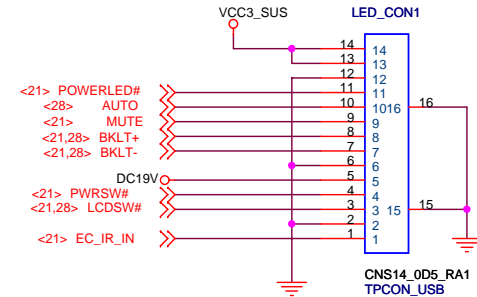
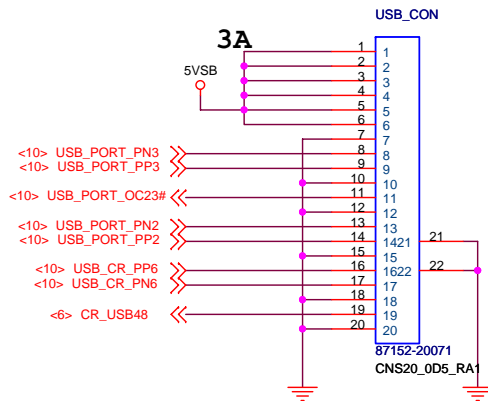
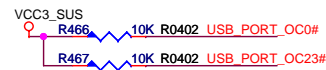
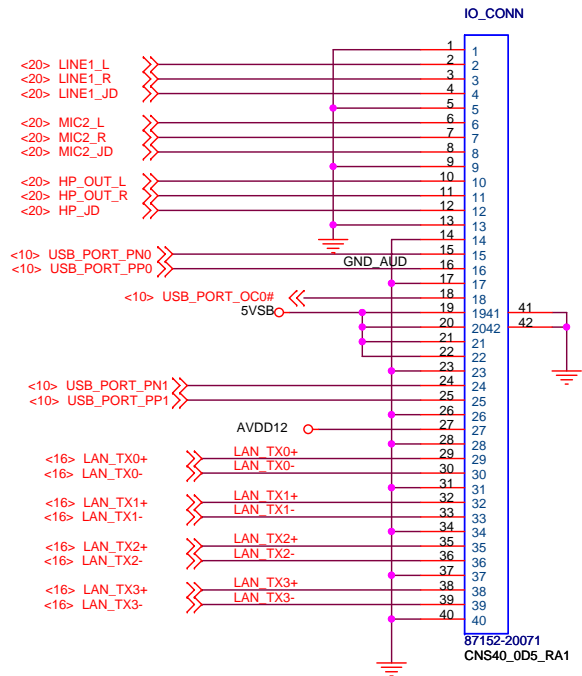
## OTP CIRCUIT



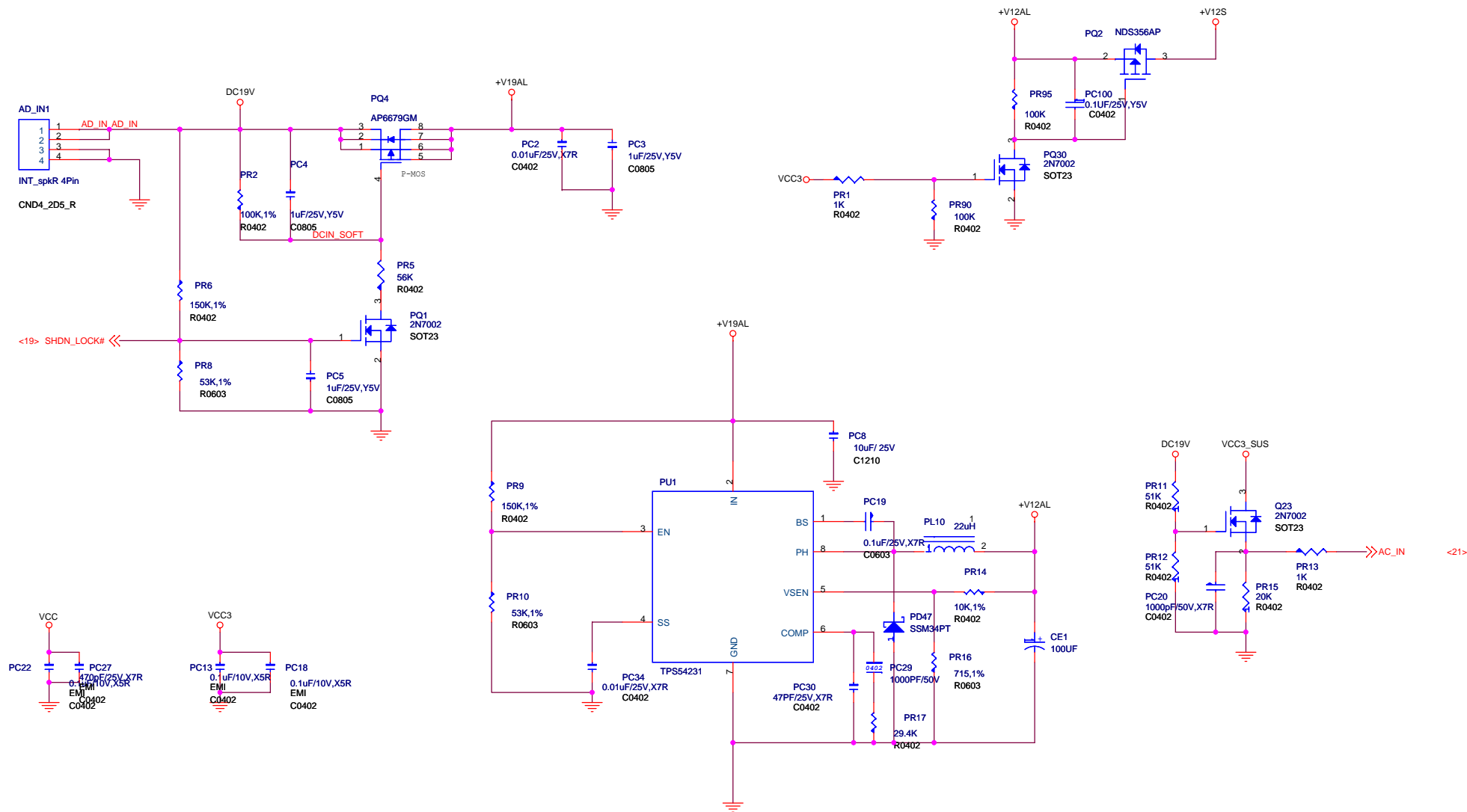
		TOPSTAR TECHNOLOGY	
Page Name		FAN/OTP	
Size B	Project Name	PINETRAIL-D	Rev A
Date:	Thursday, April 01, 2010	Sheet	19 of 31
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR			






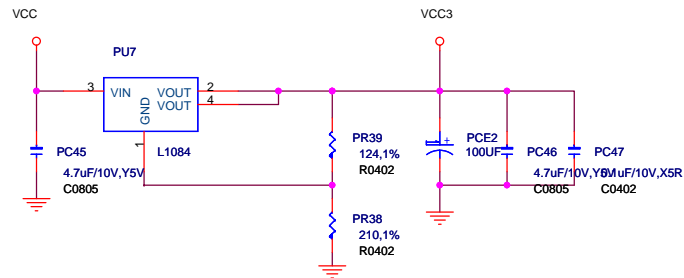
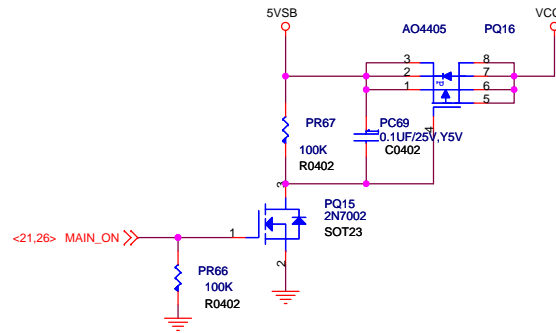
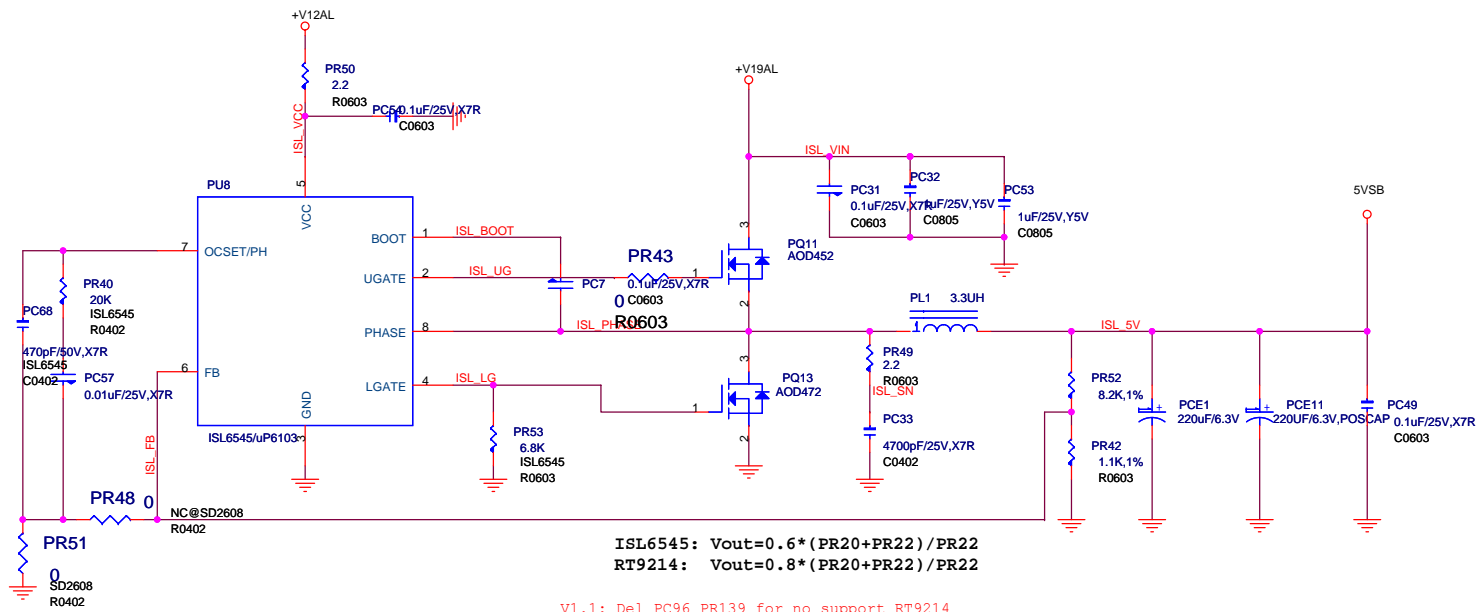


TOPSTAR TECHNOLOGY			
Page Name		DB CONN/HOLE	
Size B	Project Name	PINETRAIL-D	Rev A
Date:	Thursday, April 01, 2010	Sheet	22 of 31
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR			

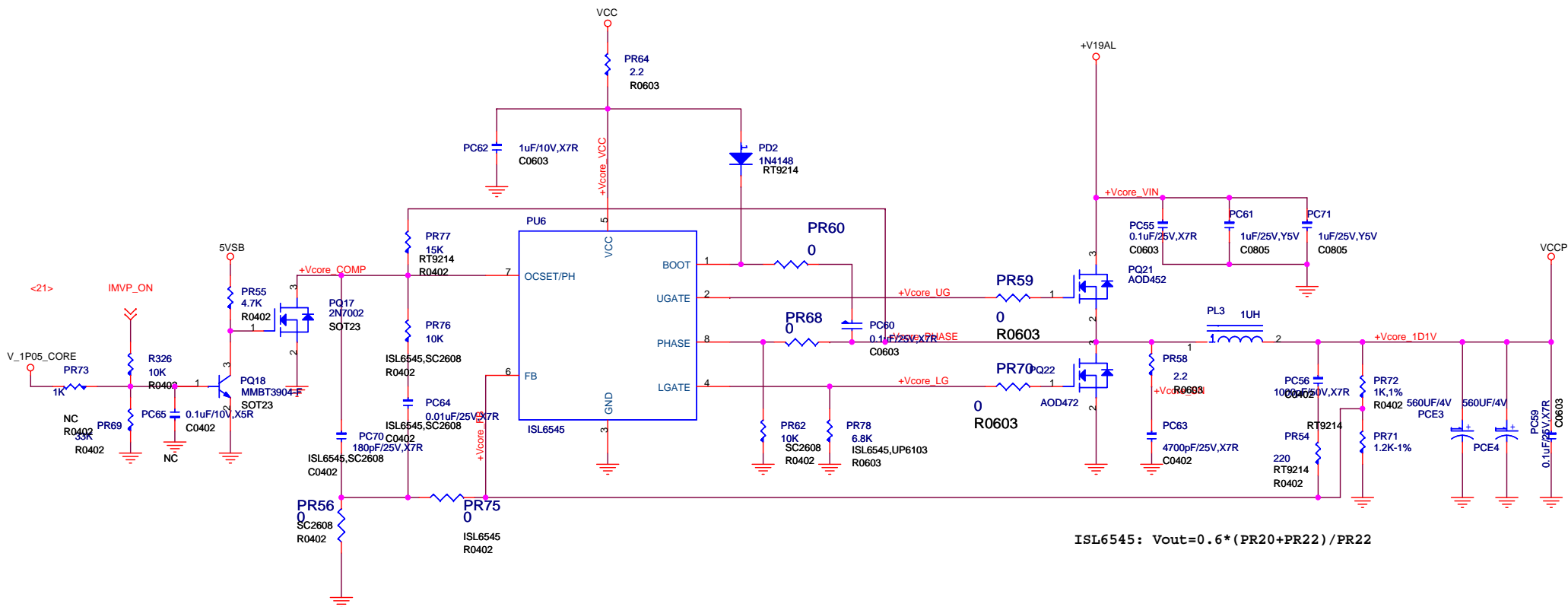


		TOPSTAR TECHNOLOGY	
Page Name		ADAPTER IN	
Size A3	Project Name	PINETRAIL-D	Rev A
Date: Thursday, April 01, 2010		Sheet 23	of 31
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR			

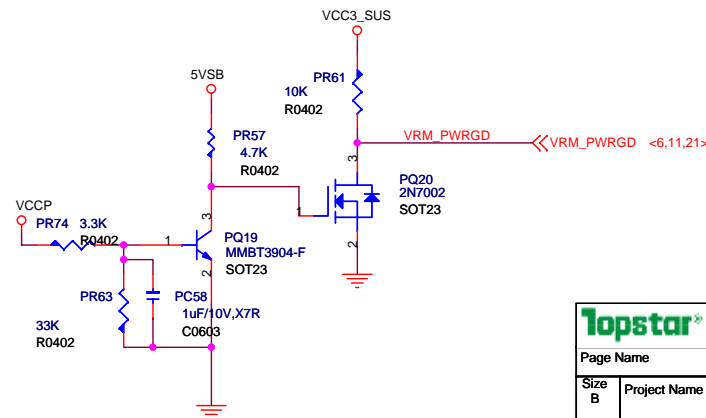
Mayc



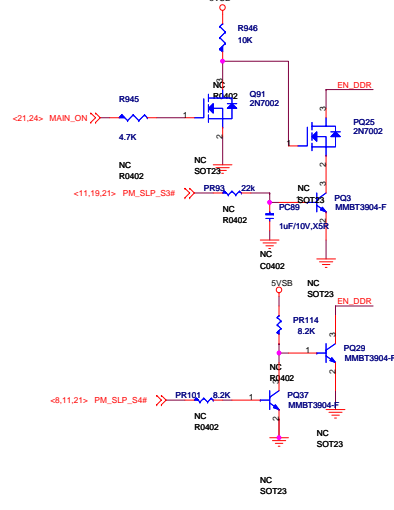
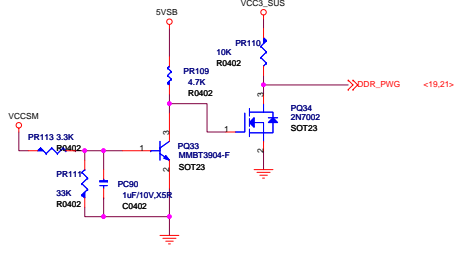
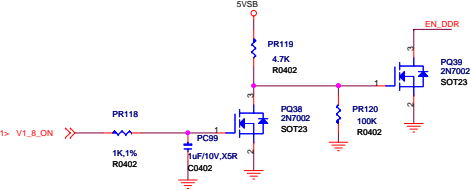
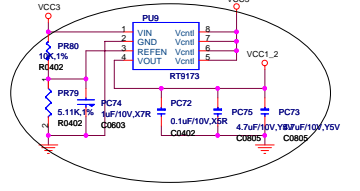
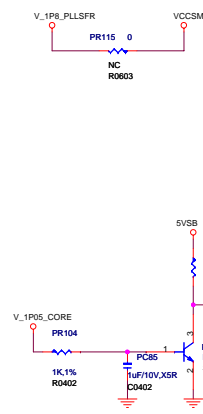
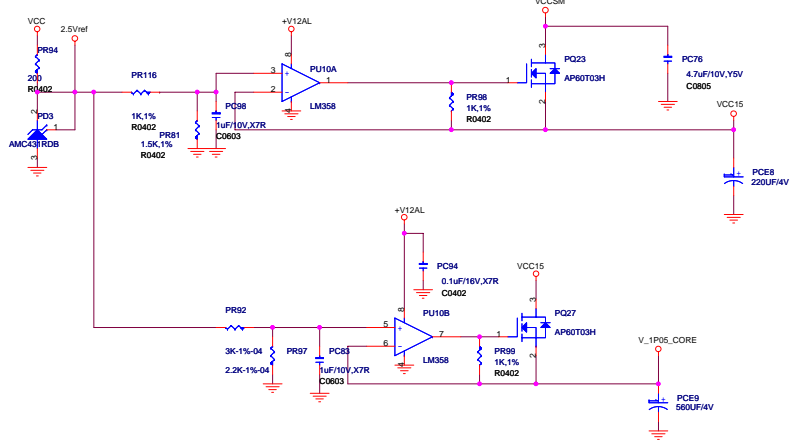
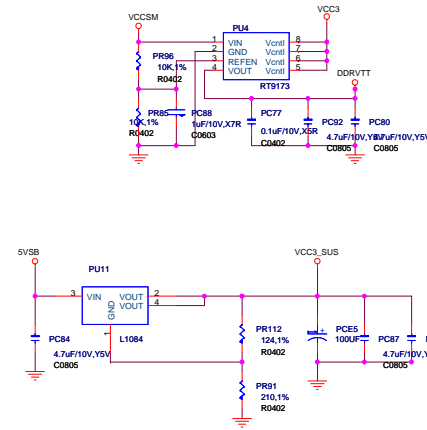
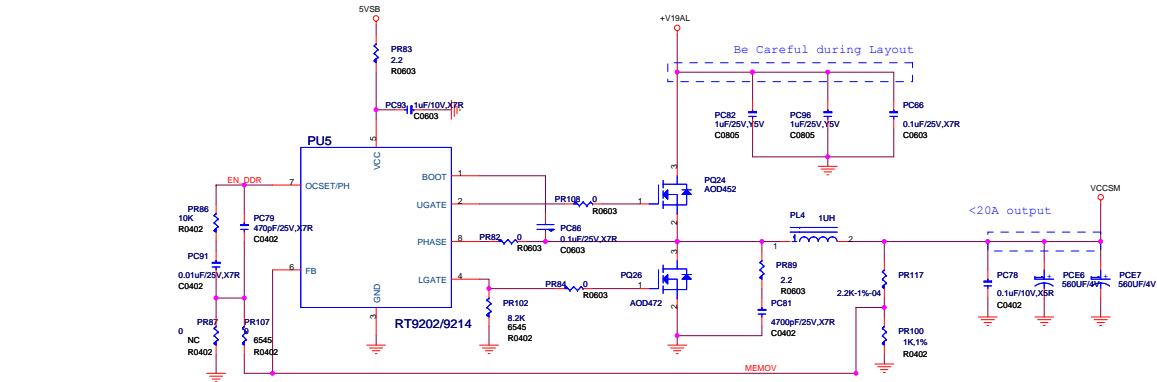


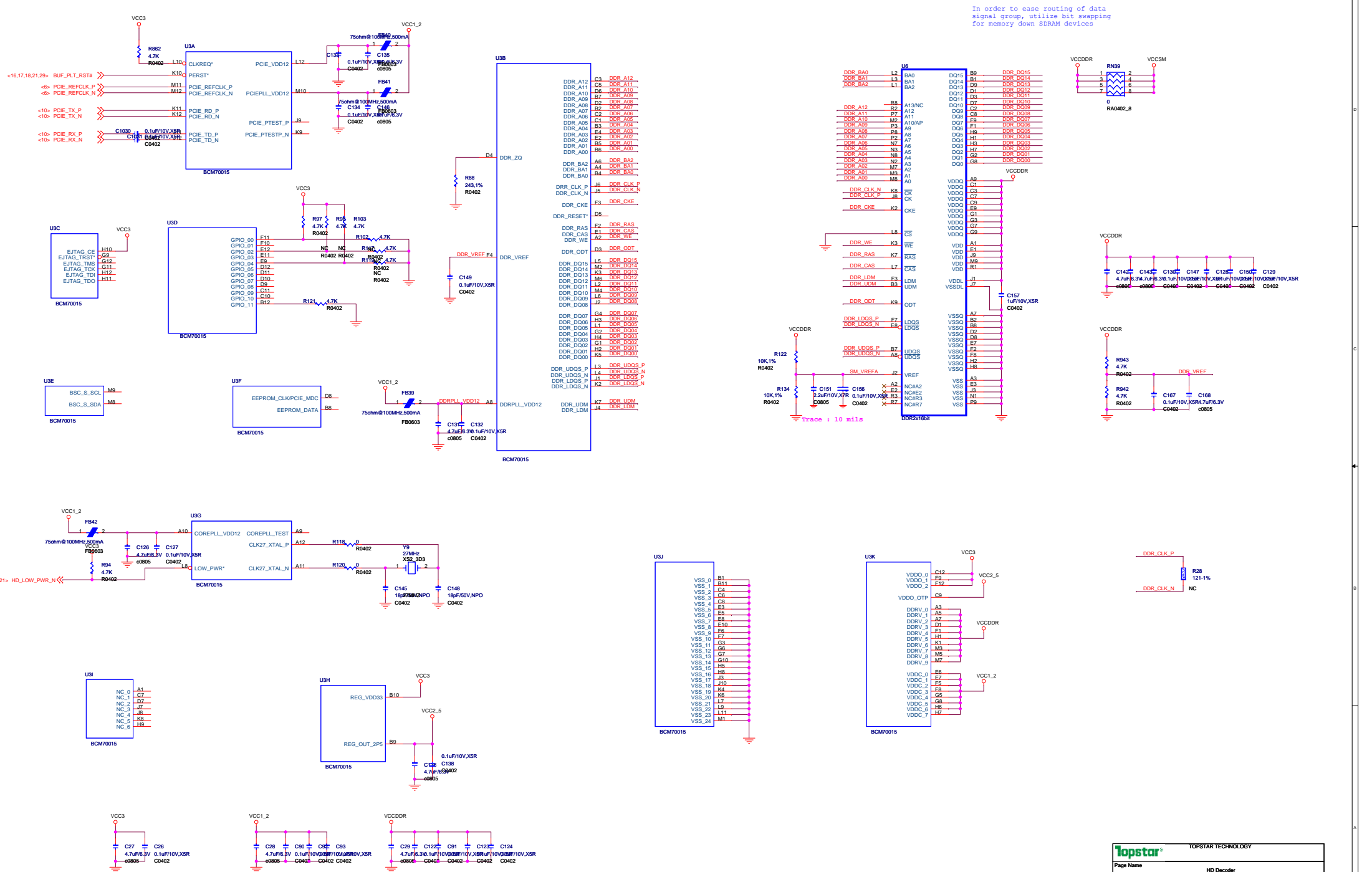


	ISL6545	UP6103	RT9214	SC2608
$I_{ocp}$	$\frac{43\mu A * R_{ocset}}{Low\_R_{ds}(on)}$		$\frac{40\mu A * R_{ocset} - 0.4V}{Low\_R_{ds}(on)}$	
Vref	0.6	0.6	0.8	0.8

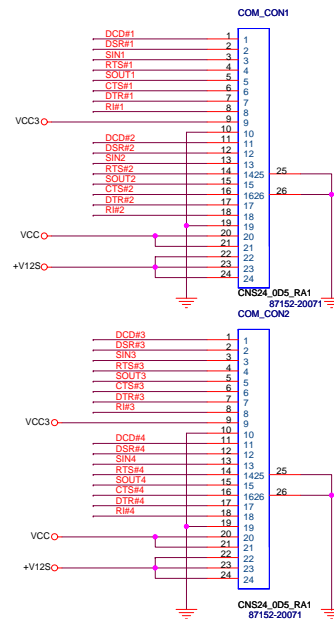
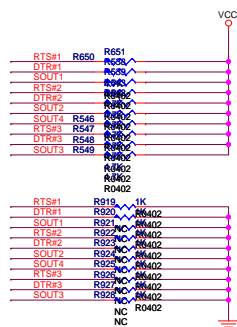
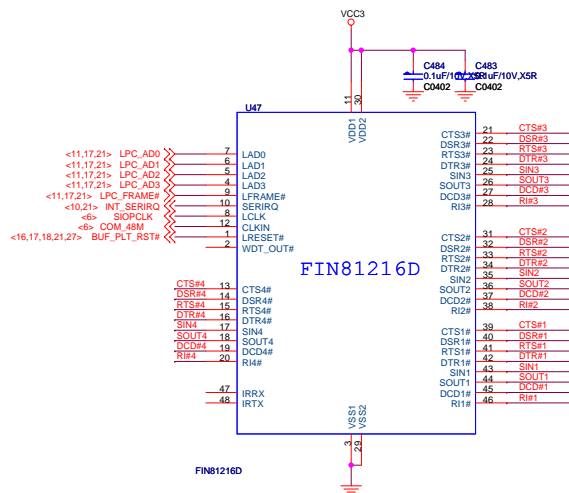


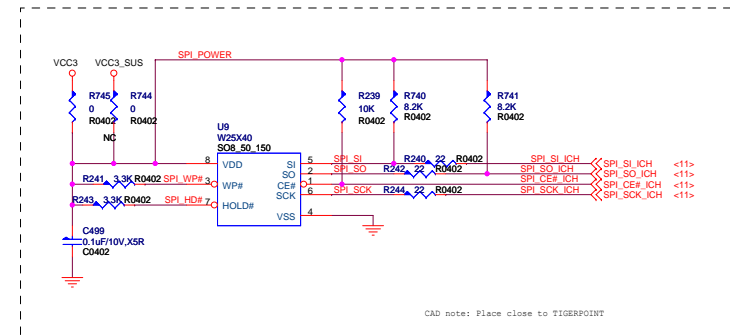
<b>Topstar</b> <sup>®</sup>		TOPSTAR TECHNOLOGY	
Page Name		+V1.8/+V0.9S DDR	
Size B	Project Name	PINETRAIL-D	Rev A
Date:	Thursday, April 01, 2010	Sheet	25 of 31
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR			



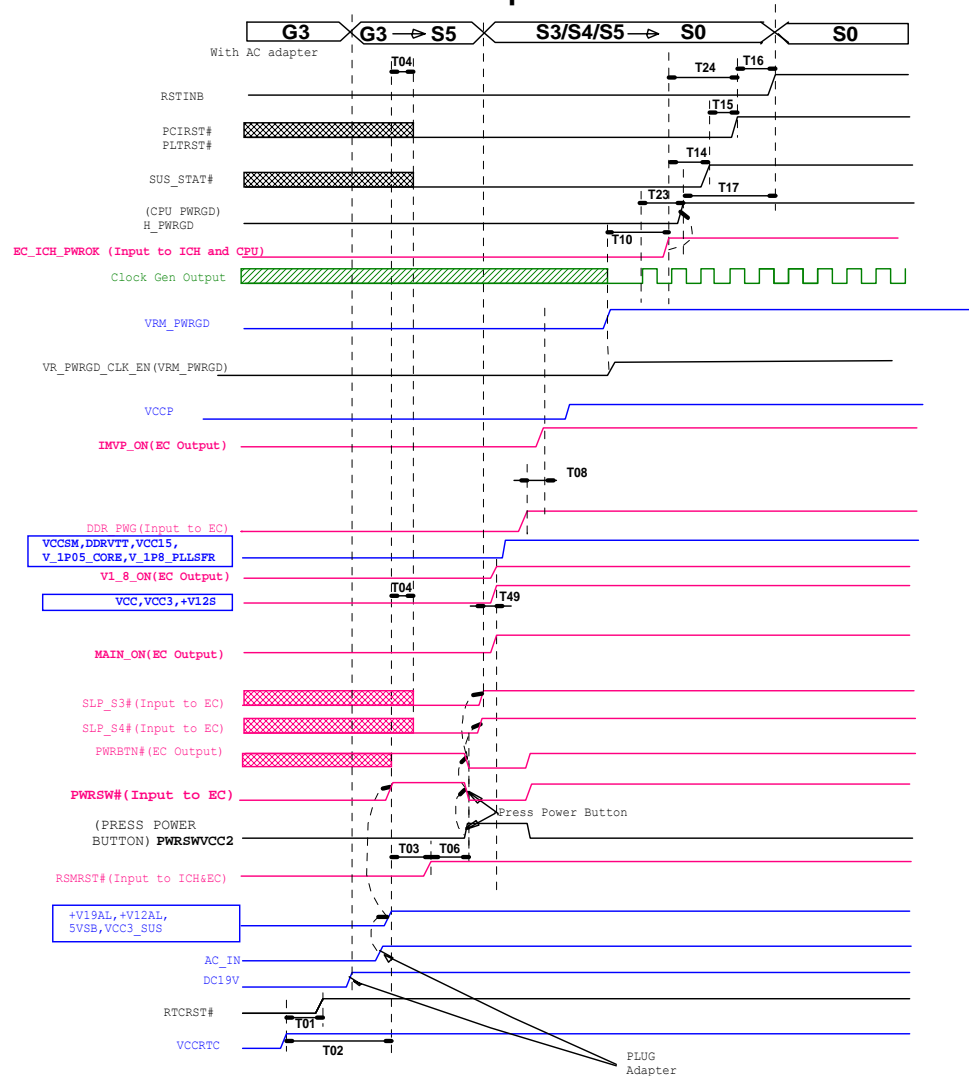




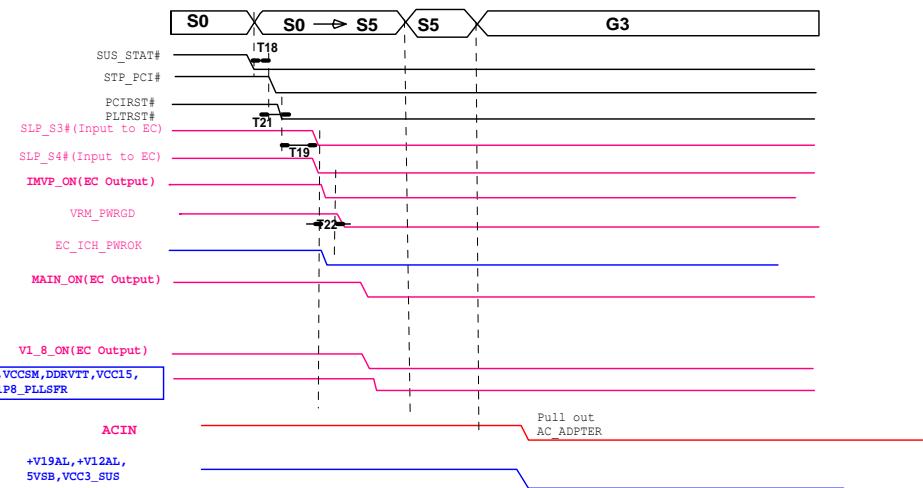




## Power On Sequence



## Power Off Sequence



<b>topstar</b>		TOPSTAR TECHNOLOGY	
Page Name		Power ON/OFF Timing	
Size	Project Name	PINETRAIL-D	Rev B
Date:	Thursday, April 01, 2010	Sheet	31 of 31
PROPERTY NOTE: this document contains information confidential and property to TOPSTAR and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained without the expressed written consent of TOPSTAR			